REMARKS

This Amendment is in response to the Office Action mailed June 23, 2003. In the Office Action, the Examiner rejected claims 1, 6, 11, and 16 under 35 U.S.C. § 112, rejected claims 1-4, 6-9, 11-14, and 16-19 under 35 U.S.C. § 102, and rejected claims 5, 10, 15, and 20 under 35 U.S.C. § 103. Applicant has canceled claims 4-5, 9-10, 14-15, and 19-20, and amended claims 1, 6, 11, and 16. Claims 1-3, 6-8, 11-13, and 16-18 remain pending in the application. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

In the specification, the paragraph that begins on page 6, line 12, has been amended to correct a minor editorial problem.

Rejection Under 35 U.S.C. § 112

The Examiner rejects claims 1, 6, 11, and 16 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner notes that the claims as presented are overly broad because they require error recovery to be performed even in the event that the memory fault indication is false. Applicant has amended the claims to correct the noted problem.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 6, 11, and 16 under 35 U.S.C. § 112, second paragraph.

Rejection Under 35 U.S.C. § 102

The Examiner rejects claims 1-2, 6-7, 11-12, and 16-17 under 35 U.S.C. § 102(b) as being anticipated by Karp et al. (US 5,748,936).

As per claim 1, applicant has amended the claim. The claim as amended includes --reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected--. A fault deferral indicator was previously claimed in claim 4, which has been canceled in view of the amendment to claim 1. The Examiner has not suggested that Karp teaches a fault deferral indication or rejected claim 4 in view of Karp.

As per claim 2, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claims 6 and 7, these claims are rejected and traversed on the same basis as discussed above for claims 1 and 2.

As per claims 11 and 12, these claims are rejected and traversed on the same basis as discussed above for claims 1 and 2.

As per claims 16 and 17, these claims are rejected and traversed on the same basis as discussed above for claims 1 and 2.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 6-7, 11-12, and 16-17 under 35 U.S.C. § 102(b) as being anticipated by Karp.

Rejection Under 35 U.S.C. § 102

The Examiner rejects claims 1, 3-4, 6, 8-9, 11, 13-14, 16, and 18-19 under 35 U.S.C. § 102(b) as being anticipated by Ross et al. (US 5,915,117).

As per claim 1, applicant has amended the claim. The claim as amended includes --reading a fault deferral indication that is true if faults can be deferred, the fault deferral indication being set before the error in the memory is detected--. A fault deferral indicator was previously claimed in claim 4, which has been canceled in view of the amendment to claim 1. The Examiner asserted that Ross teaches of a fault deferral indicator citing the teaching of the IPSR.ed bit in column 11, lines 30-33. The fault deferral indicator as now claimed in claim 1 is set before an error is detected. The IPSR.ed bit taught by Ross is set by the operating system (Fig. 2, 212; col. 10, line 66, to col. 11, line 15) when control is passed from the exception handler (Fig. 1, 110; col. 8, lines 57-61) after an error is detected. Ross does not teach a fault deferral indicator as now claimed. Claim 1 has been further amended to state that the method receives and retains control of the machine after a memory error occurs until control is returned to the executing program. The method taught by Ross generates an exception into the operating system (Fig. 1, 110; col. 8, lines 57-61) which distinguishes the method of Ross from the now claimed invention.

As per claim 3, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

As per claim 4, this claim is canceled.

As per claims 6, 8, and 9, these claims are rejected and traversed on the same basis as discussed above for claims 1, 3, and 4.

As per claims 11, 13, and 14, these claims are rejected and traversed on the same basis as discussed above for claims 1, 3, and 4.

As per claims 16, 18, and 19, these claims are rejected and traversed on the same basis as discussed above for claims 1, 3, and 4.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 3-4, 6, 8-9, 11, 13-14, 16, and 18-19 under 35 U.S.C. § 102(b) as being anticipated by Ross.

Rejection Under 35 U.S.C. § 103

The Examiner rejects claims 5, 10, 15, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Ross et al. (US 5,915,117).

Applicant has canceled claims 5, 10, 15, and 20.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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